I hereby certify that this correspondence is being sent by the United States Postal Office via Express Mail Certificate No. : ER046066927Us and is addressed to : Commissioner of Patents and Trademarks, Alexandria, VA 22313, on June15 2004. The applicant and/or attorney requests the date of deposit as the filing date. Depositor: Karen Cinq-Mars

Karen Cinq-Mars 6/15/04
(Signature & date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of :	June 15 2004
Bruce B. Doris, et al :	Group Art No: 2818
Serial No. 10/604,190 :	Examiner: David Vu
Filed: 6/30/03 :	IBM Corporation Bldg. 300, Zip 482 2070 Route 52 Hopewell Junction, NY 12533
Title: HIGH PERFORMANCE CMOS DEVICE STRUCTURES AND METHOD OF MANUFACTURE :	

TITLE: HIGH PERFORMANCE CMOS DEVICE STRUCTURES AND METHOD OF MANUFACTURE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

If any fees are required for this submission, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Bruce B. Doris, et al.

By Joseph P. Abate 6-15-04
Joseph P. Abate
Registration No. 30,238
Telephone No. 845-894-4633

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
FIS920030152US1	10/604,190
Applicant(s)	
Bruce B. Doris, et al.	
Filing Date	Group Art Unit
6/30/03	2818

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Novel Locally Strained Channel Technique for High Performance 55nm CMOS K. Ota, et al. 2002 IEEE, 2.2.1-2.2.4, IEDM 27. Local Mechanical-Stress Control (LMC): A New Technique for CMOS - Performance Enchancement A. Shimizu, et al. 2001 IEEE, 19.4.1-19.4.4, IEDM 01-433
		Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design Shinya Ito, et al. 2000 IEEE, 10.7.1-10,7.4, IEDM 00-247 A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System -on-a- Chip Applications F. Ootsuka, et al. 2000 IEEE, 23.5.1-23.5.4, IEDM 00-575

EXAMINER	DATE CONSIDERED

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		NMOS Drive Current Reduction Caused by Transistor-Layout and Trench Isolation Induced Stress Gregory Scott, et al. 1999 IEEE, 34.4.1-34.4.4, IEDM 99-827
		Transconductance Enhancement in Deep Submicron Strained-Si n- MOSFETs Kern (Ken) Rim, et al. 1998 IEEE, 26.8.1-26.8.4, IEDM 98-707
		Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFET's K. Rim, et al. 2002 IEEE, 98-99, 2002 Symposium On VLSI Technology Digest of Technical Papers

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